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D. Remarks

Rejection of Claims 10, 14-16 and 19 Under 35 U.S.C. §102(a) based on Applicant's Background Art (*Background Art*).

The invention of claim 10 is directed to a method of forming a monitoring structure. The method includes etching a first layer to form monitor trenches that extend through the first layer and stop at an etch stop layer on a monitor wafer. The method also include forming a feature in, with, or in relation to the monitor trenches, wherein a process to be monitored with said monitor structure forms a corresponding non-monitor trench in a different layer or material than the first layer.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. Because the *Background Art* does not show all limitations of claim 10, this ground of rejection is traversed.

Applicants' *Background Art* shows two conventional monitoring processes. Neither of these conventional examples forms a monitoring trench in first layer, and then forms a non-monitoring trench in a different layer or material than the first layer. Applicants' first example shows the monitoring of a chemical mechanical polishing step by forming monitoring trenches in a substrate.[1] The process to be monitored forms trenches in the same layer and material. That is, the first example forms trenches in a substrate to monitor a process that forms trenches in the same substrate. Accordingly, the first example of the *Background Art* cannot show a process to be monitored that forms a non-monitor trench in a different layer or material than a first layer.

Applicants' second example does not show any trench formation. Applicants' second example describes monitoring a silicon-on-insulator (SOI) structure. However, no trenches are ever described as being formed. Clarification of where trench formation is mentioned with regard to FIG. 8 is respectfully requested.

Further, the second example describes using an SOI structure having silicon

[1] See Applicants' Specification, Page 2, Lines 22-23, which describe trench formation for both monitor trenches and non-monitor trenches, and Page 3, 17-19, which describes how a wafer (having the monitor trenches) is removed from a process to serve as a monitor wafer.

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islands formed thereon as a monitoring structure, to monitor a process that forms the same structure (i.e., not a structure having trench formed in a different layer or material).

If it is being argued that the two examples are being combined to sustain the rejection, such a combination is untenable. The first example describes the formation of a shallow trench isolation structure. The second example describes an SOI structure. As is well understood in the art, SOI structures are utilized to avoid STI or LOCOS type isolation.

Accordingly, because the *Background Art* does not show all limitations of claim 10, this ground of rejection is traversed.

Claim 15, which depends from claim 10, has additional limitations not shown in the cited reference. Nothing in the reference shows or describes an etch mask that essentially matches an SOI wafer island isolation pattern. The *Background Art* shows but one etch mask, and the etch mask matches a shallow trench isolation pattern, not any SOI island isolation pattern.[2]

Accordingly, the *Background Art* does not show all the limitations of claim 15, either.

For all of these reasons, this ground of rejection is traversed.

Rejection of Claims 20 and 23-25 Under 35 U.S.C. §102(a) based on the *Background Art*.

The invention of claim 20 is directed to a method of monitoring a semiconductor manufacturing process. The method includes processing a monitor wafer having monitoring trenches formed in a first layer of the monitoring wafer according to at least one process step that forms a feature, the feature being formed in a non-monitoring wafer in, with, or in relation to a different layer than the first layer in the semiconductor manufacturing process.

To address this ground of rejection, Applicants incorporate by reference herein the same general comments set forth above for claim 10. Namely, that the *Background Art* does not show a monitor wafer with monitoring trenches in one layer that monitors a process that forms a feature in a different layer. In particular, both examples from the *Background Art* show a monitor wafer having identical structures to that formed by the monitored process.

[2] See Applicants' Specification, FIGS. 5A and 5B.

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Claim 10 has been amended, not in response to the cited art, but to address, but to more clearly define the invention.

The present claims 10-26 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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